Control of ion flux-energy distribution at dielectric wafer surfaces by low frequency tailored voltage waveforms in capacitively coupled plasmas

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Abstract

Capacitively coupled plasmas are routinely used in an increasing number of technological applications, where a precise control of the flux and energy distribution of ions impacting boundary surfaces is required. In the presence of dielectric wafers and targets the accumulation of charges on these surfaces can significantly alter the time evolution of the sheath electric field that is accountable for ion acceleration from the plasma bulk to the surfaces and, thus, lead to parasitic distortions of process relevant ion flux-energy distributions. We apply particle in cell with Monte Carlo collisions simulations to provide insights into the operation, ion acceleration mechanisms, and the formation of such distributions at dielectric wafers for discharges in argon gas. The discharges are driven by a combination of a single high frequency (HF) (27.1 MHz) voltage signal and a low frequency (LF) (100 kHz) customized pulsed voltage waveform. The LF waveform includes a base square signal to realize narrow and controllable high energy peaks of the ion distribution, and steady-slope ramp voltage components. We discuss the distorting effect of dielectric surface charging on the ion flux-energy distribution and provide details about how the voltage ramps can restore its narrow peaked shape. The dependence of the surface charging properties on the LF pulse duty cycle and amplitude, as well as the HF voltage amplitude is revealed. The radial homogeneity of the ion flux is found to be maintained within $\pm 10\%$ around the mean value for all quantities investigated. The radial electric field developing at the edge of the dielectric wafer with finite width has only a small influence on the overall homogeneity of the plasma across the whole surface, its effect remains localized to the outermost few mm of the wafer.

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1. Introduction

Low pressure capacitively coupled radio frequency discharges (capacitively coupled plasmas (CCPs)) are frequently utilized for the treatment of various kinds of surfaces in high-tech applications. The modification of the surface can involve etching, implantation, thin film deposition, cleaning, sterilization, modification of wettability or biocompatibility properties, etc [1–3]. The operation principle is based on the generation of reactive atomic/molecular particles in the gas phase, followed by their transport to the target surface. Depending on the specific properties of the filling gas a large variety of plasma-chemical reaction channels can contribute to the creation of the radicals but, in general, it starts with free electrons in the plasma that acquire significant kinetic energy through power absorption from the applied radio frequency (RF) electric field [4–6]. In the case of charged plasma particles, the transport from the bulk region is governed by the RF sheath that develops in front of boundary surfaces. In the case of positively charged ions, the typical RF period, on the order of 10–100 ns, is too short with respect to the ion sheath transit time, and the ions effectively react to the time averaged electric field. Negative ions are efficiently confined to the plasma bulk by the sheath electric field, and both their creation by electron attachment and loss by neutralization occur in the bulk region. The electrons, on the other hand, are light and mobile, respond to the RF electric field, and can have large enough kinetic energy to overcome the residual sheath electric field during phases of sheath collapse. Modern applications, like atomic layer deposition or removal, which represent a high degree of chemical selectivity, often require a detailed control of the flux and the energy distribution of ions arriving at the surface [7, 8]. To realize atomic layer precision narrow peaks of the ion flux-energy distribution function (IFEDF) at the wafer with controllable energies are required in many cases [8]. Such control of the IFEDF can be achieved through the modulation of the sheath electric field (or sheath voltage) at time scales that are comparable or longer than the ion transit time. Over the past decades, several techniques have been developed, which have in common that those go beyond the single frequency symmetric voltage drive. Asymmetric tailored driving voltage waveforms can be achieved based on the combination of carefully adjusted subsequent harmonic RF components (called Fourier ansatz) [9–11] or by using a superposition of a single high frequency (HF) component to drive plasma generation, and a low frequency (LF) modulation signal of arbitrary shape with a repetition rate as low as 10–100 kHz to control the sheath voltage evolution [12–18]. In case of square-shaped voltage waveforms and in the presence of a conducting wafer, the presence of a broad plateau of the applied voltage waveform leads to the formation of a narrow peak of the IFEDF at the

wafer surface at low pressure, since the sheath voltage remains constant for a large fraction of the pulse period. The position of this peak on the energy axis can be controlled by adjusting this plateau value [17, 18].

The target/wafer surfaces can be conductive or dielectric. In the case of conductive surfaces, the voltage drop across the discharge gap can be fully controlled by the external driving electrical circuit and essentially no voltage drops across the target/wafer itself. In our earlier study, we have shown that with a customized voltage waveform, composed of a 27.12 MHz HF component and a pulsed, square waveform with 100 kHz repetition rate, a significant flux of high energy ions can be produced in large area CCPs. With the variation of the voltage pulse amplitude and duty cycle, the flux and energy of these ions can be tuned with high precision [18].

In the case of dielectric targets (e.g. Si wafers in microelectronics, glass or quartz substrates in solar panel fabrication) the periodic charging of the 'wafer' surface (as we will refer to it in the following) can significantly alter the voltage drop across the discharge. A significant fraction of the applied voltage drops across the charged wafer reducing the voltage drop across the plasma [13, 19, 20]. Furthermore, the charge state of the dielectric surface, depending on the specific wafer material, can significantly influence the plasma particle impact induced secondary electron emission probabilities, as it was discussed recently [21]. The secondary electron emission yields, including both electron and ion impact induced processes, can significantly affect the discharge properties, especially at high voltage and low pressure conditions, most relevant to etching applications [22]. In the case of tailored voltage waveforms the time dependent voltage drop across the charged dielectric wafer can, in principle, be fully compensated with a properly tuned waveform, however, the shape of the required correction depends on the individual properties of each experiment. In the case of HF sine + LF square pulsed voltage waveform an additional, variable slope voltage ramp on the positive or the negative part of the LF pulse has been shown to efficiently compensate the voltage drop on the wafer, reestablishing the narrow energy distribution of the ion flux to the wafer in a remote inductively coupled plasma (ICP) source experiment [17]. An equivalent circuit model was developed to explain the operation of this source including the dynamical charging of the dielectric wafer [23]. Additional experiments confirmed the operation details by measuring the time resolved flux-energy distribution of the impacting ions [24]. Recent studies target the homogeneity over large area surfaces of both the total flux and the angular distribution of the impacting ions [25].

In this numerical study, we focus on low pressure argon CCPs driven with a superposition of a single frequency 27.1 MHz cosine and a pulsed voltage waveform including

linear voltage ramps in addition to the principle square pulses. The system includes a simple capacitor model for the dielectric wafer, which is placed on one of the (powered or grounded) electrodes. One dimensional (1d3v = 'one dimensional in real space and three dimensional in velocity space') particle in cell with Monte Carlo collisions (PIC/MCCs) simulations are used to discuss the fundamental operation principles and parameter variations. In this way the time dependent charging of a dielectric wafer exposed to the plasma, the resulting voltage drop across it, and the IFEDF distortion are computed. Based on this results, we demonstrate that the inclusion of a ramp into the tailored driving voltage waveform can compensate this IFEDF distortion and restore the desired narrow-peaked shape of the ion distribution function at the wafer surface. In addition, two dimensional (2d3v) axisymmetric PIC/MCC simulations are applied to investigate the effect of the geometrical asymmetry on the plasma parameters and the radial distribution of the charging and ion flux across the wafer surface. The motivation for this study is to provide a high level of control of the IFEDF at the dielectric wafer surface, similarly to our previous study on conductive targets [18], which provides further insights into the operation of such pulsed CCPs.

2. PIC/MCC simulations

The primary tool of the present study is our graphic processing unit (GPU) accelerated electrostatic PIC/MCC simulation code, which follows the traditional PIC/MCC scheme developed for collisional plasmas and implemented in various flavors by several research groups [26–33]. A detailed description of the present model and its one dimensional sequential implementation can be found in our earlier publication [34], while the GPU acceleration and optimization strategies are introduced separately [35]. The implementation of the two dimensional axisymmetric simulation is discussed in previous works [5, 36]. Therefore, here we detail only the implementation of the dielectric wafer into our 1d3v and 2d3v simulations and define the applied voltage waveforms.

In the simplest implementation of the dielectric wafer the radial distribution of the charged particle fluxes at the surfaces is neglected and, from the perspective of the electrical circuit, it can be represented by its capacitance C_{wafer}. The wafer can be placed either at the grounded side or on top of the powered electrode, as shown in figures 1(a) and (b). In both cases, the voltage drop across the discharge gap $V_{\mathrm{gap}}(t)$ is the difference between the supplied voltage $V(t)$ and the voltages dropping on the blocking capacitor $V_{\mathrm{block}}(t)$ and the wafer $V_{\mathrm{wafer}}(t)$. Usually, the blocking capacitor has a capacitance in the 100 nF range, large enough to develop negligible voltage variation within one RF cycle and to effectively decouple the DC voltage levels of the electrode and the power supply without altering the AC voltage components. On the other hand, the wafer capacitance is a function of the wafer properties, approximated by the parallel plate capacitor model as $C_{\mathrm{wafer}} = \varepsilon_0 kA/d$, where k is the material dependent dielectric constant, A is the
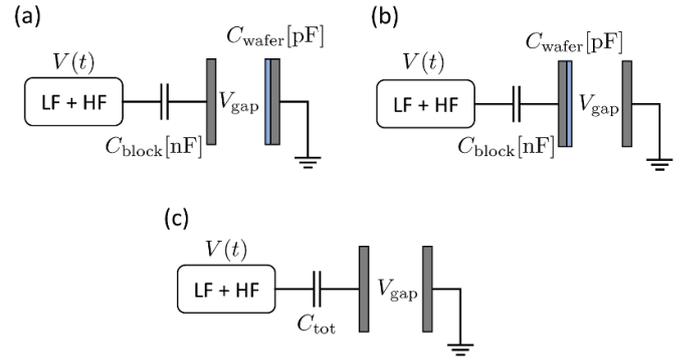
Figure 1. Sketches of the possible system configurations with the dielectric wafer at the grounded side (a) and on the powered electrode (b). The simplified equivalent circuit (c) combines the external blocking capacitor C_{block} and the wafer capacitance C_{wafer} into C_{tot}.

plasma facing surface area, and d is the width of the wafer. For example, a 5 mm thick glass wafer has a capacitance per surface area of approx. $1\,\mathrm{pF\,cm^{-2}}$, a 1 mm thick Si wafer has a capacitance per surface area of approx. $10\,\mathrm{pF\,cm^{-2}}$, etc typically significantly smaller than C_{block}. In this simple circuit model, the blocking and wafer capacitors are connected in series, they experience the same charging currents, and, therefore, regardless of the wafer position, the circuit can be simplified by combining the capacitors into a single series capacitor as $C_{\mathrm{tot}} = C_{\mathrm{wafer}} \times C_{\mathrm{block}}/(C_{\mathrm{wafer}} + C_{\mathrm{block}}) \approx C_{\mathrm{wafer}}$ as shown in figure 1(c). The calculation of the time-dependent voltage drop on the combined capacitance is implemented in the simulations following the algorithm introduced in [37] by counting individual charged particle fluxes to and from the plasma-facing surfaces. Besides the charging, both surfaces are characterized by the same surface coefficients for the $\mathrm{Ar^+}$ ion-induced secondary electron emission with constant yield $\gamma = 0.1$, and elastic electron reflection with a constant probability $\eta = 0.5$.

From the perspective of plasma generation, the only relevant voltage is $V_{\mathrm{gap}}(t) = V(t) - V_{\mathrm{wafer}}(t) = V(t) - Q_{\mathrm{wafer}}(t)/C_{\mathrm{wafer}}$, depending on the applied voltage, $V(t)$, and the charge state of the wafer, computed self-consistently in the simulations. The supplied voltage waveform is a superposition of a $f_{\mathrm{HF}} = 27.1\,\mathrm{MHz}$ cosine wave with $V_{\mathrm{HF}} = 92\,\mathrm{V}$ amplitude and a pulsed signal with $f_{\mathrm{LF}} = 100\,\mathrm{kHz}$ repetition rate. An example of the LF signal is shown in figure 2 and it is characterized by a constant voltage rise time $t_{\mathrm{rise}} = 200\,\mathrm{ns}$, a duty cycle D, defined as the ratio of the full width at half maximum of the positive voltage pulse in the LF waveform and the full LF period length, and a peak-to-peak voltage $V_{\mathrm{LF,pp}}$ of the base square signal. Additionally, linear voltage ramps can be switched on at the positive (high) and the negative (low) voltage portions of the LF signal, characterized by the ramp voltages V_{rp} and V_{rn}, respectively. Experimentally, such ramped voltage waveforms can be generated by power supplies that have been developed for such types of Voltage Waveform Tailoring [17].
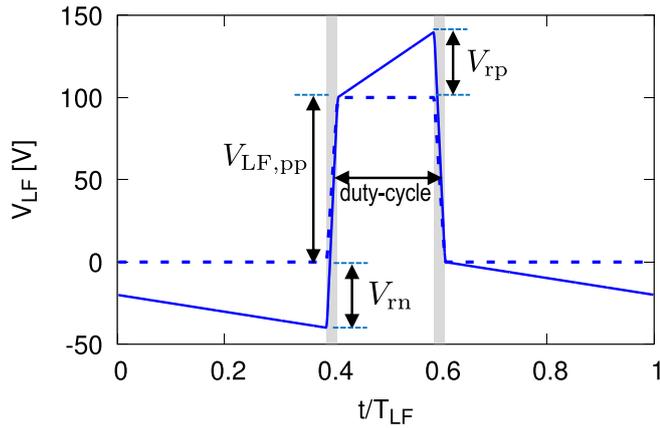
Figure 2. Example of the low frequency pulsed voltage waveform. The principal squared voltage pulse, as shown with dashed lines, is characterized by the repetition rate $f_{LF} = 100$ kHz, the peak-to-peak voltage $V_{LF,pp}$, the duty cycle D, and the voltage rise time ($t_{rise} = 200$ ns, indicated by the shaded ranges). The final LF voltage waveform, as shown with solid lines, includes optional linear voltage ramps on the positive and negative portions.

Figure 3. Sketches of the 2d3v PIC/MCC model geometries. The dielectric wafer can be placed on the powered electrode (a) or the grounded side (b). The wafer is modeled as a set of individual capacitors placed at every grid point (c). The width of the wafer is neglected in most runs, except for the cases dedicated to the edge effect, where it is assumed to be $d = 2$ mm.

The simulations are performed in 1 Pa argon gas, the discharge gap is 75 mm, and the gas temperature is set to a constant 350 K. In the 1d3v PIC/MCC case the numerical grid has a resolution of 512 grid points, and a superparticle weight of 40 000 is used (assuming a nominal electrode area of 1 cm^2) which resulted in approx. 600 particles per cell for each species (electrons and Ar$^+$ ions). A time step of approx. 10 ps is used, which is enough to fulfill the usual stability criteria expected from the PIC/MCC scheme, as discussed in detail in [38].

In the case of the axisymmetric 2d3v PIC/MCC simulations, the implemented geometry follows our previous work and is based on the multiple frequency CCP (MFCCP) chamber operating at the Department of Electrical Engineering and Information Science, Ruhr-University Bochum [18, 39]. In this case, the 300 mm diameter wafer is modeled as a set of individual capacitors placed on the bottom flat electrode, which could be powered or at ground potential, as shown in figure 3. The horizontal electrodes have diameters of 492 mm and are separated in radial direction by 1 mm gaps from the outer cylindrical grounded metallic wall. The width of the dielectric wafer is neglected by default, however, for a single case dedicated to the effect of the wafer edge electric field, it is assumed to be $d = 2$ mm. An equivolumetric numerical grid with 1024×1024 points is used for the collection of individual particle properties, like the construction of the charge density distribution. This is followed by an interpolation of the particle distributions to an equidistant grid to solve Poisson's equation employing successive over-relaxation iterations and the electrostatic force calculation.

The reason for the application of both 1d3d and 2d3v PIC/MCC simulations in a single study is that the significantly faster 1d3v simulations allow parametric scans to be performed in a reasonable time while giving valuable insights into the operating principles of the discharge system. The running times of 2d3v simulations can be up to 50 times longer than
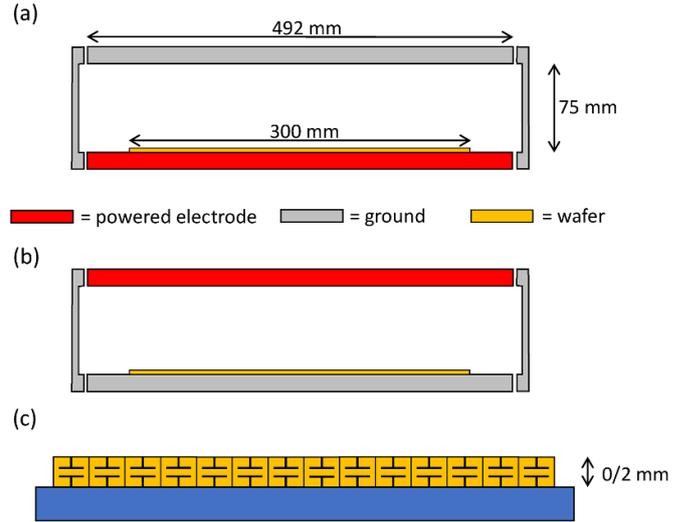
the 1d3v counterparts, but provide information on the radial distribution of particle fluxes and incorporate the geometrical asymmetries often significant in experimental systems.

3. Discharge operation (1d3v simulations)

3.1. The base case

First, we define a reference base case which we discuss in detail, and parameter variations will be performed with respect to this case. Common geometry, gas, surface, and numerical parameters (identical for all cases) have been defined above, the electrical parameters defining the base case are: $V_{HF} = 92$ V, $V_{LF,pp} = 100$ V with $D = 20\%$ duty cycle and ramp voltages $V_{rp} = V_{rn} = 0$ V. For consistency, this case is chosen to be identical to the base case of our previous study on IFEDF control featuring conductive electrodes [18]. The effect of the dielectric wafer is implemented following the simplified equivalent circuit model as shown in figure 1(c) with $C_{tot} = C_{wafer}$.

Figure 4 shows the HF averaged time evolution of the driving voltage waveform V_{PS} and the gap voltage V_{gap} for three different values of the wafer capacitance per surface area, $C_{wafer} = 1, 10,$ and 100 pF cm^{-2}. We note that the real voltage waveform contains 271 full cycles of the HF voltage oscillation. However, including those in the plots would greatly decrease the visibility of the relevant features, therefore now and in the following the voltages shown in the figures are averaged over the individual HF oscillation and are denoted as LF voltage waveforms.

For the case with the highest wafer capacitance, the charging currents during the different portions of the LF waveform have little effect on the voltage drop on the wafer, the gap
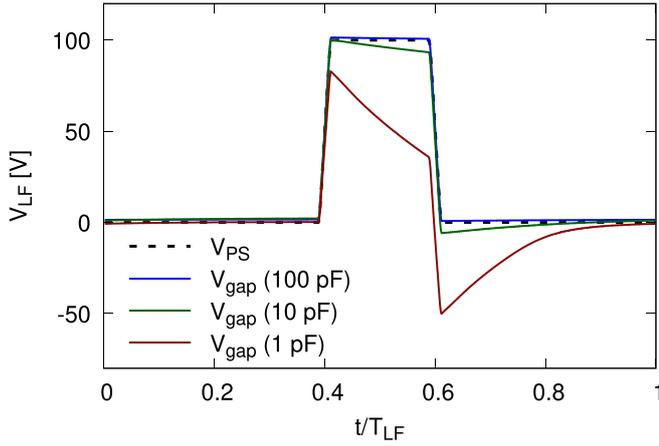
Figure 4. Low frequency component (averaged over the individual HF periods) of the gap voltages for the base case with C_{wafer} values between 1 and $100\,\mathrm{pF\,cm^{-2}}$. The applied voltage waveform provided by the power supply, corresponding to the base case, V_{PS}, is shown with a dashed line.

voltage closely follows the waveform generated by the power supply V_{PS}, only a slight DC shift can be observed, which develops in all cases ensuring the long time averaged zero DC current requirement. For smaller wafer capacitances, however, the net conduction currents to the wafer from the plasma cause significant distortions to the voltage drop across the electrode gap due to time dependent charging of the dielectric. This occurs because part of the applied voltage drops on the charged dielectric wafer itself. More precisely, it results in a lack of an extended high (positive or negative) constant voltage period in the LF gap voltage, which has direct consequences on the IFEDF at the wafer due to its effects on the time dependent sheath voltage at the wafer, as shown in figure 5.

Figure 6 shows the time resolved IFEDFs at the grounded side for the reference simulation case with $C_{wafer} = 100\,\mathrm{pF\,cm^{-2}}$ (a), and $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$ (b). In the case of high wafer capacitance, the formation of two plateaus within each LF period is observed, resulting in two sharp peaks in the time averaged IFEDF, with the high energy peak being populated during the short positive voltage pulse. The low energy peak is a consequence of the time averaged HF sheath voltage at the wafer. For many applications, especially those requiring atomic layer precision, such narrow and controllable high energy peaks of the IFEDF are desirable. Any widening of this peak and/or generation of ions at intermediate energies can result in a loss of selectivity and, thus, atomic layer precision as the ion energy window for such precision is left [8]. In the case of low wafer capacitance, this is exactly what happens due to wafer charging, i.e. the ion energy distribution during the short positive voltage pulse does not remain steady. This is caused by the gradual decrease of the gap voltage at the microsecond time scale as more voltage drops across the dielectric wafer. The persistent surface charging results in a decreasing difference between the bulk plasma potential and the surface potential, which is responsible for the acceleration of the positive ions from the plasma bulk to the surface.
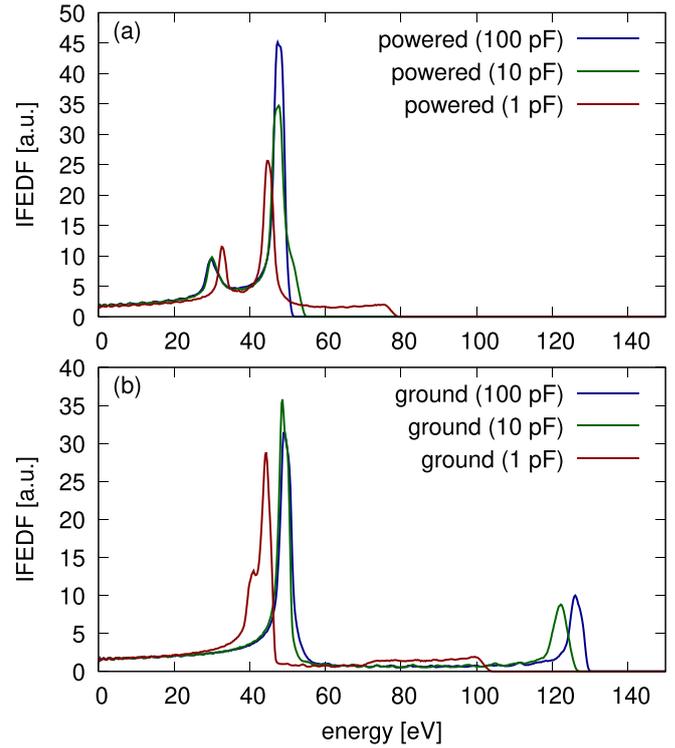

Figure 5. IFEDFs at the powered (a) and the grounded electrodes (b) for $C_{wafer} = 100\,\mathrm{pF\,cm^{-2}}$, $C_{wafer} = 10\,\mathrm{pF\,cm^{-2}}$, and $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$.
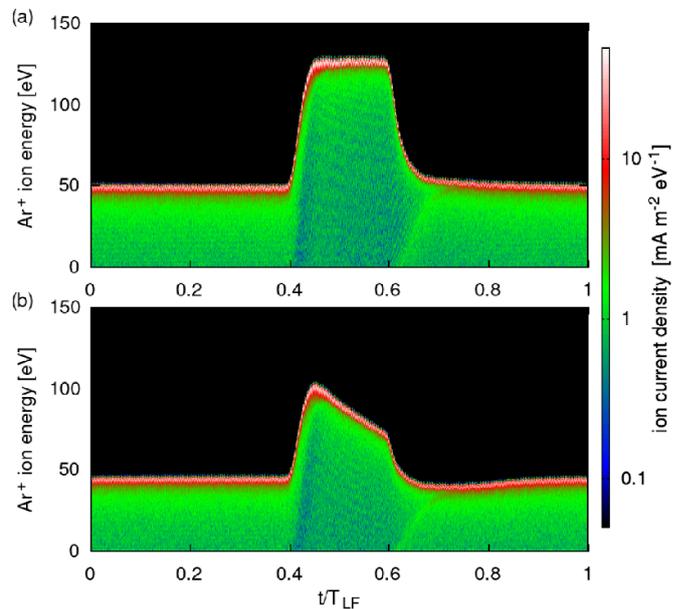
Figure 6. Computed time resolved IFEDF at the grounded electrode for $C_{wafer} = 100\,\mathrm{pF\,cm^{-2}}$ (a), and $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$ (b). The other discharge parameters correspond to the base case.

In the case of high wafer capacitance, $C_{wafer} \geqslant 100\,\mathrm{pF\,cm^{-2}}$, the discharge characteristics are identical with the conductive electrode cases as studied previously [18]. In this case, for low duty cycles, $D < 40\%$, a well-defined peak develops in the IFEDF at the grounded electrode,
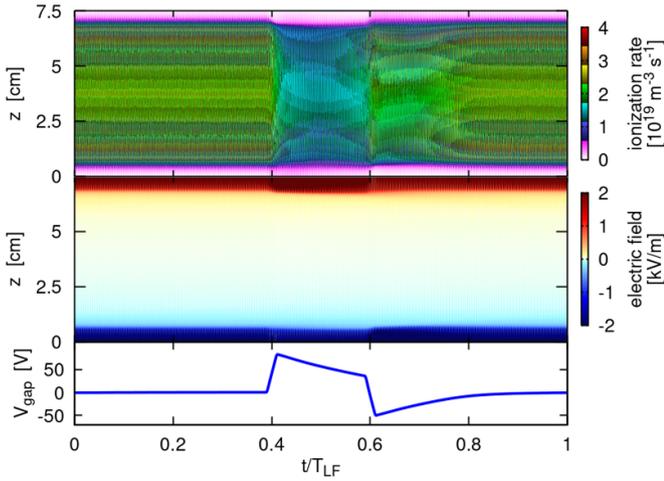
Figure 7. Spatio-temporal evolution of the ionization rate and electric field distributions as well as the time evolution of the low-pass filtered gap voltage. Base case with $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$.

Figure 8. Species resolved HF averaged current densities at the powered (a) and grounded (b) electrodes, as well as the charge state of the series capacitor (c). Base case with $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$. The shaded area indicates the period of the positive voltage pulse.

at approx. 125 eV, while the IFEDF at the powered side contains only low energy features and a sharp cutoff, at approx. 50 eV. The IFEDFs are very different in the case of $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$. The high energy peak at the grounded side becomes blurred and displaced towards lower energies, while at the powered electrode the IFEDF develops a low intensity plateau extending towards higher energies.

As, from the cases introduced so far, the $C_{wafer} = 1\,\mathrm{pF\,cm^{-2}}$ case shows the most significant effect of the dielectric wafer both on the discharge voltage evolution and the IFEDFs, in the following our analysis will focus on this scenario. It is to note that the discharge currents during the different phases of the HF cosine waveform give rise to measurable voltage variation on such a low series capacitance, effectively reducing the applied HF voltage amplitude V_{HF} by approx. 8%. This does primarily influence the plasma generation, slightly lowering the bulk plasma density, no significant effect on the IFEDF is found, therefore this phenomenon is not further discussed. The aim of this study is to show that with the addition of properly adjusted linear voltage ramps to different sections of the applied LF voltage waveform the effect of wafer charge variation can be compensated and the sharp high energy peak in the IFEDF can be restored.

To provide deeper insights into the operation of the reference discharge, figure 7 shows spatio-temporal distributions of the ionization source and the electric field in relation to the evolution of the gap voltage. Before the positive voltage pulse, the discharge is in a stationary operation regime, characterized by a symmetric field structure and high ionization rates governed by the HF excitation through HF sheath expansion heating of electrons [40]. During the positive pulse the discharge symmetry is broken, the sheath adjacent to the grounded electrode (at $z = 7.5$ cm) does not fully collapse at any phase of the HF voltage oscillation, while the sheath at the powered electrode gets shorter, allowing the rapid drain of electrons through this surface. Consequently, the ionization rate is reduced. After
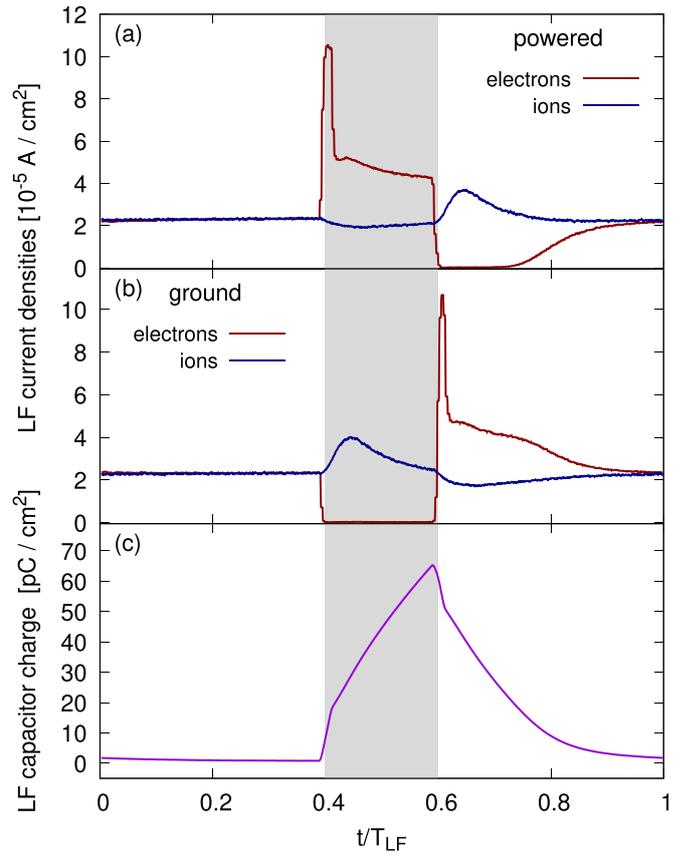
the positive voltage pulse the roles of the electrode sheaths gets reversed, the sheath at the powered side (at $z = 0$ cm) remains extended for several HF oscillations, effectively blocking the plasma electrons from reaching the surface, while attracting ions towards the electrode. It takes approx. $2\,\mu s$ after the pulse to recover to the stationary operation regime.

Figure 8 shows the charged particle current densities at the powered and grounded sides of the discharge and the resulting charge state of the series capacitor, representing the dielectric wafer in the system. As discussed above, during the positive voltage pulse the permanently expanded RF sheath at the grounded side repels all electrons arriving from the plasma bulk at the grounded side attracting the positive ions at the same time. In contrast to this, at the powered side, the RF sheath partially collapses, which causes a strong imbalance of charged particle fluxes, resulting in significant net currents charging the series capacitor. The slope of the capacitor charge variation is determined by two principal factors. Due to the small electrons' inertia, during the steep voltage transitions, the electrons react almost instantly, a short (on the order of the voltage rise time t_{rise}) and large amplitude current pulse passes through the collapsing sheath, that result in a quick voltage jump on the capacitor. After this transient, the charging is governed by the slower ion dynamics, resulting in a nearly linear
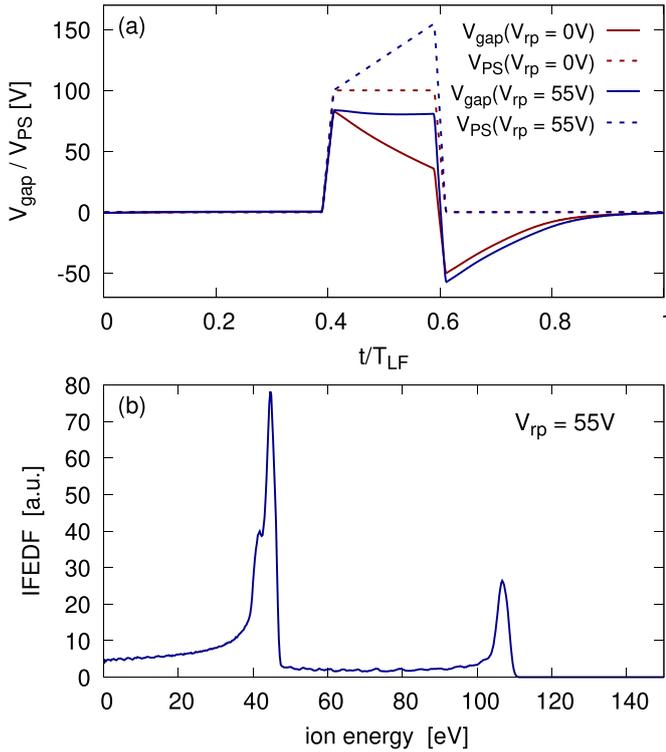
Figure 9. (a) HF filtered gap voltages for the base case with $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$ with and without positive ramp voltage. The input voltage waveforms provided by the power supply V_{PS} are shown with dashed lines. (b) IFEDF at the grounded electrode with the addition of $V_{\text{rp}} = 55\,\text{V}$ to the base case voltage waveform.

Figure 10. Duty cycle variation of the HF averaged charge evolution on the wafer with $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$, $V_{\text{HF}} = 92\,\text{V}$, and $V_{\text{LF,pp}} = 100\,\text{V}$, $V_{\text{rp}} = 0\,\text{V}$.
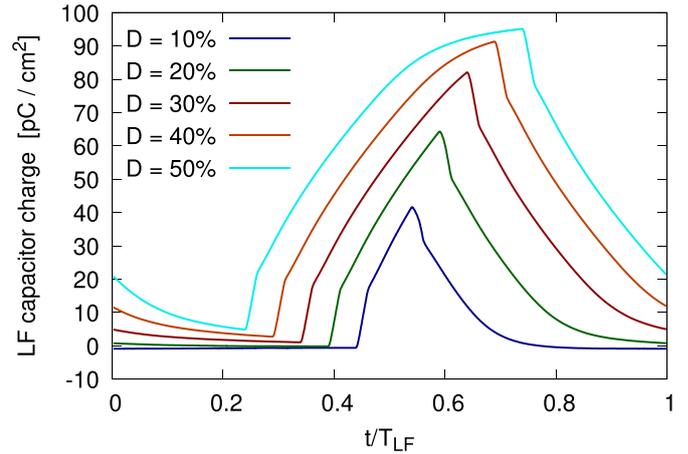
capacitor charge variation, until the stationary state is reached again.

Based on these insights on the wafer charging and its relation to the time evolution of the IFEDF we can assume that by adding a positive voltage ramp to the positive LF voltage pulse we should be able to compensate the increasing voltage drop on the wafer (series capacitor) and resume the high and stable acceleration of bulk ions towards the wafer surface.

Figure 9 supports the concept of this study. The shape of the positive LF voltage pulse could be restored in the gap voltage, although the amplitude is reduced with respect to the applied voltage waveform, as seen in panel (a). This is caused by the large amplitude nanosecond transient charging currents appearing at the rising and falling edges of the voltage pulse, as discussed in figure 8. Nevertheless, the flat high voltage plateau in V_{gap} ensures the steady acceleration of ions towards the grounded side, resulting in the restoration of the high energy peak in the IFEDF even in the presence of a strong voltage drop across a charged dielectric wafer. This can be seen in the panel (b), where the peak forms at approx. 20 eV lower energy compared to the high C_{wafer} case, as shown in figure 5.

3.2. Duty cycle variation

As already discussed in our previous study, the duty cycle is a key parameter to control the IFEDF at the electrodes [18]. At

low duty cycles, $D < 40\%$, a population of high energy ions is formed at the grounded side in increasing quantities but with a fairly constant energy with increasing D. The range $40\% < D < 50\%$ is a transition region, where the position of the high energy peak in the IFEDF moves quickly to lower values with increasing D. Due to the intrinsic symmetry of the one dimensional geometry approximation, the range $D > 50\%$ is a mirror image of the $D < 50\%$ regime with the large ion acceleration now at the powered electrode side. For this reason, we restrict most of our discussions in this section to $D < 50\%$, as all relevant statements made for this regime are valid for $D > 50\%$ as well with the exchange of V_{rp} by V_{rn} and 'grounded side' by 'powered side'.

Figure 10 shows the HF filtered time evolution of the charge state of the series capacitor with capacitance $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$ and discharge conditions otherwise identical with the base case, as defined above. Clearly, the longer positive LF voltage period does induce charging currents that last longer and, therefore, the series capacitor (the wafer) does acquire more charges and higher voltage, however, the amplitude of the charging current, equivalent to the slope of the charge evolution, does not depend on the duty cycle, unless saturation is reached, as it can be seen for $D = 50\%$. This means, that the compensation for the wafer charging should be possible with a D independent voltage slope, or in other words with $V_{\text{rp}} \propto D$ in a fairly broad range of D.

Figure 11 shows the IFEDFs for different duty cycles with ramp voltages that were individually iterated (in steps of 5 V) to provide the sharpest high energy peaks. The optimum V_{rp} values follow the above formulated expectation for its D dependence.

3.3. LF voltage variation

In the ideal case of complete separation of the plasma generation (driven by the HF voltage) from the ion energy control (provided by the tailored LF voltage waveform) the bulk

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P Hartmann *et al*
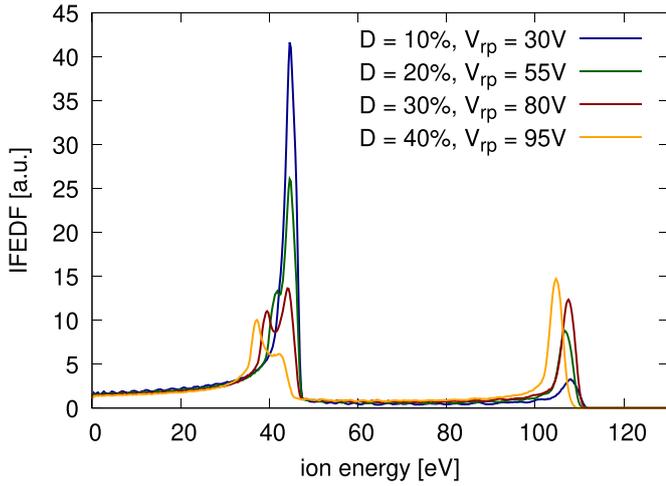
Figure 11. Duty cycle variation of the IFEDFs with optimal ramp voltages. Discharge parameters are $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$, $V_{\text{HF}} = 92\,\text{V}$, and $V_{\text{LF,pp}} = 100\,\text{V}$.

plasma properties should not depend on the amplitude of the LF voltage pulse. In fact, the peak electron density reduces only by approx. 5% while changing $V_{\text{LF,pp}}$ from 100 V to 500 V. This suggests that the capacitor charging currents should also be comparable for otherwise identical discharge conditions.

Figure 12(a) shows the HF filtered time evolution of the gap voltage for different values of $V_{\text{LF,pp}}$ with $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$ and otherwise base case identical discharge conditions. With increasing $V_{\text{LF,pp}}$ the amplitude of the voltage pulse in V_{gap} increases proportionally, however, the slope of the observed voltage decay during the voltage pulse varies only by a smaller fraction. Panels (b) and (c) compare the IFEDFs at the grounded side for a series of different $V_{\text{LF,pp}}$ values with $V_{\text{rp}} = 0\,\text{V}$ (b) and $V_{\text{rp}} = 50\,\text{V}$ (c). Apparently, in the non-compensated cases, the high energy peaks are all blurred, but can fairly well be resumed by using a single value of the ramp voltage, regardless of the LF voltage peak amplitude.

3.4. HF voltage variation

The situation is very different in the case of HF voltage variation, as this is expected to significantly influence the plasma generation. In fact, as figure 13(a) shows, the peak electron density in the plasma bulk does vary by a factor of 3 while changing V_{HF} from 60 V to 120 V. As a consequence, the surface charging currents at the wafer are expected to be significantly different even for otherwise identical discharge conditions.

Figure 13(b) shows the IFEDFs for different values of V_{HF} for $V_{\text{LF,pp}} = 200\,\text{V}$, $V_{\text{rp}} = 50\,\text{V}$, $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$, and $D = 20\%$ conditions. It is apparent that the broadening of the high energy peak cannot be compensated with a single ramp voltage for different HF voltage amplitudes, the narrowest spectral peak is recovered only for $V_{\text{HF}} = 92\,\text{V}$. The observed width of the high energy peak increases as the
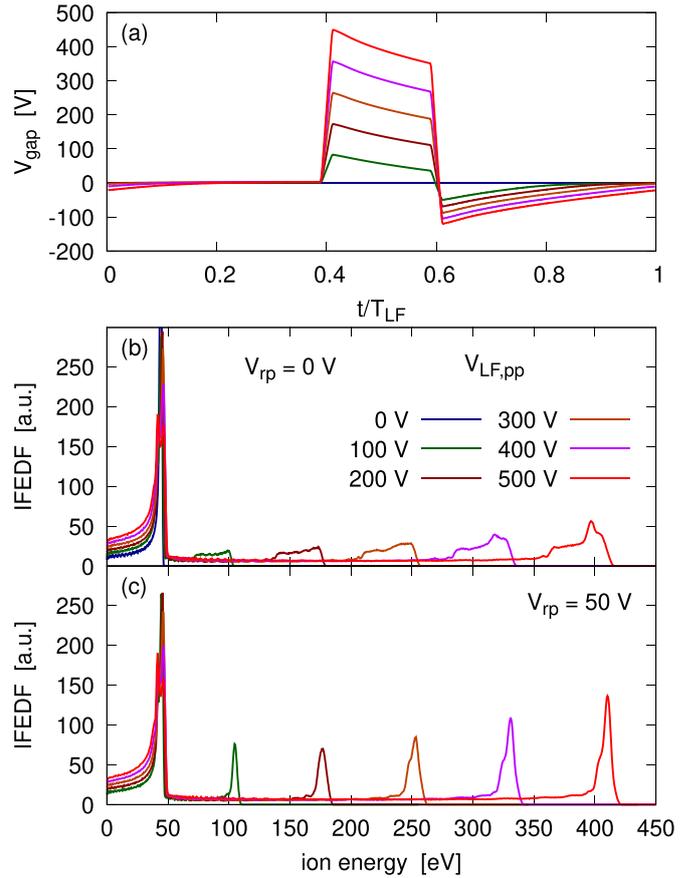

Figure 12. Time evolution of the gap voltage for different values of $V_{\text{LF,pp}}$ (a). IFEDFs for the same set of $V_{\text{LF,pp}}$ without voltage ramp (b) and with $V_{\text{rp}} = 50\,\text{V}$ (c). $C_{\text{wafer}} = 1\,\text{pF}\,\text{cm}^{-2}$ with otherwise base case identical discharge conditions.

difference between the applied V_{HF} and its optimum value is increased. The ramp voltage needs to be adjusted individually for every value of the HF voltage amplitude to restore the desired IFEDF shape. In contrast to previous cases, the total ion flux ($\int f_{\text{IFEDF}}(\varepsilon)\,\text{d}\varepsilon$) does increase significantly with increasing V_{HF}, causing the observed inability of a single voltage ramp to compensate the surface charging for all V_{HF} values. The position of the low energy peak in the IFEDF is directly determined by the time-averaged sheath potential during the off-pulse period, which is in connection with the total ion flux through the Child–Langmuir law in this collisionless sheath regime.

4. Radial distributions (2d3v simulations)

So far we have seen that applying pulsed LF voltage waveforms with $D < 40\%$ and $V_{\text{rp}} > 0\,\text{V}$ allows effectively compensating the charging of a dielectric wafer placed on the grounded electrode, while with $D > 60\%$ and $V_{\text{rn}} > 0\,\text{V}$ the same is possible for a wafer at the powered side. As a result, the aimed high energy peak in the corresponding IFEDFs could be recovered. Due to the intrinsic symmetries of the 1d3v PIC/MCC simulations, these two scenarios could be discussed

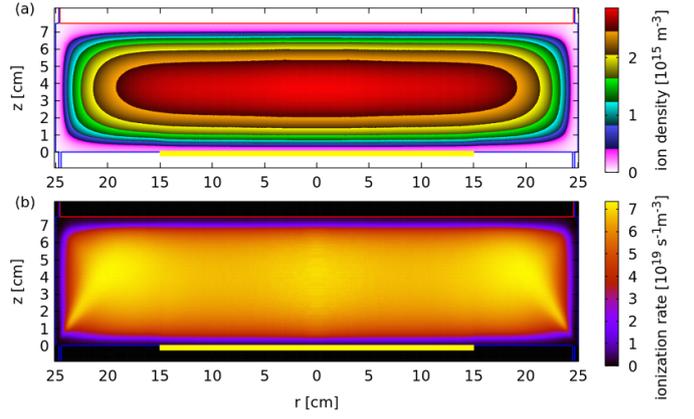J. Phys. D: Appl. Phys. **56** (2023) 055202

P Hartmann *et al*
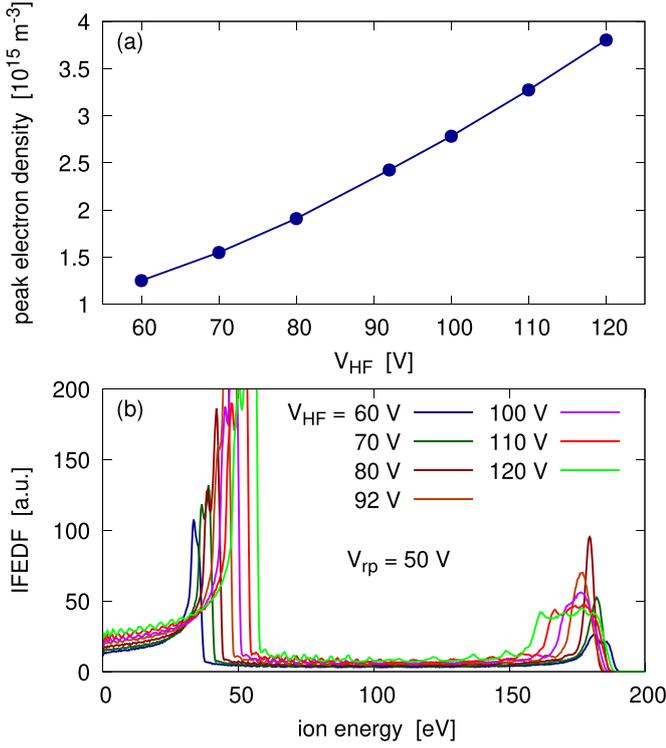
Figure 13. Peak electron density vs. HF voltage amplitude (a). IFEDFs for the listed values of the HF voltage amplitude with a constant value of the ramp voltage $V_{rp} = 50$ V. Discharge conditions include: $V_{LF,pp} = 200$ V, $D = 20\%$, $C_{wafer} = 1$ pF cm^{-2}.


Figure 14. Spatial distribution of the time averaged Ar$^+$ ion density (a) and the ionization rate (b). Powered and grounded conductive surfaces are outlined with red and blue lines, respectively. The wafer with $C_{wafer} = 1$ pF cm^{-2} is marked with a thick yellow line embedded into the lower (grounded) electrode. The voltage waveform parameters are: $V_{LF,pp} = 100$ V, $D = 20\%$, $V_{rp} = 85$ V, and $V_{HF} = 92$ V.

in a uniform manner. Extending the model with an additional spatial dimension to a 2d3v axisymmetric simulation makes it possible to describe the experimentally more relevant geometries, including the typical asymmetry between the electrically powered and grounded plasma facing surfaces. As we have shown in our previous study, the statements drawn based on 1d3v simulations remain qualitatively valid, the actual numerical values, however, become somewhat shifted, and the $D < 50\% \leftrightarrow D > 50\%$ mirrored equivalence is not exactly true [18] due to an additional DC self-bias voltage that develops as a consequence of the geometrical asymmetry.

In this section, we discuss the spatial distribution of some plasma generation, and IFEDF relevant quantities, as well as the effect of the geometrical edge of the wafer with finite thickness. The geometry is adapted from the MFCCP experiment, as it was introduced in figure 3. To keep the amount of information shared in a manageable extent, we restrict the discussions to the cases, derived from the base case, where the best compensation of the wafer charging regarding the recovery of the high energy peak in the IFEDFs was achieved.

4.1. Wafer on the grounded side

The discharge conditions are: $V_{HF} = 92$ V, corresponding to 60 W RF power input in previous experiments, $V_{LF,pp} = 100$ V, $V_{rp} = 85$ V, $C_{wafer} = 1$ pF cm^{-2}, and $D = 20\%$. The wafer thickness is neglected, it is placed on the grounded electrode,

and its radius (15 cm) is smaller than the metallic electrode, requiring different boundary conditions for the grid points with different radial coordinates. For $r < 15$ cm the surface charge in every grid cell, and with this the electric potential is computed individually, while for $r > 15$ cm the applied potential is used as a boundary condition, allowing for the development of the DC self-bias voltage.

Figure 14 shows the time-averaged Ar$^+$ ion density distribution in panel (a) and the time-averaged distribution of the ionization source function in panel (b). The density has a structure typical for low pressure CCPs, where the density maximum develops in the center, and falls off rapidly approaching any of the confining surfaces. Charged particles in the gas phase are created primarily by electron impact ionization from the neutral Ar buffer gas. The spatial distribution of this process's rate is fairly homogeneous in the plasma bulk, however, a weak local maximum can be seen at the outer radial position. This is a consequence of the superposition of the HF sheath expansion dynamics at the horizontal (electrode) and vertical (wall) grounded surfaces, as discussed in earlier works [5]. This supports the assumption that, under these conditions, the discharge operates in the sheath expansion heating regime, also called α-mode.

Figure 15 shows the time evolution of the radial distribution of the surface charge density across the dielectric wafer. Before the positive voltage pulse, the surface charge is negligibly small and constant in time. During the LF pulse, topped with a significant voltage ramp, the wafer surface charges up gradually, but no significant radial inhomogeneity can be seen. Only after the falling edge of the voltage pulse, at the outermost few millimeters of the wafer, the de-charging of the dielectric shows a somewhat slower rate.

A fair degree of radial homogeneity can be seen in the radially resolved IFEDF data with only small deviations, as shown in figure 16. The IFEDFs are acquired for every decade of

J. Phys. D: Appl. Phys. **56** (2023) 055202

P Hartmann *et al*
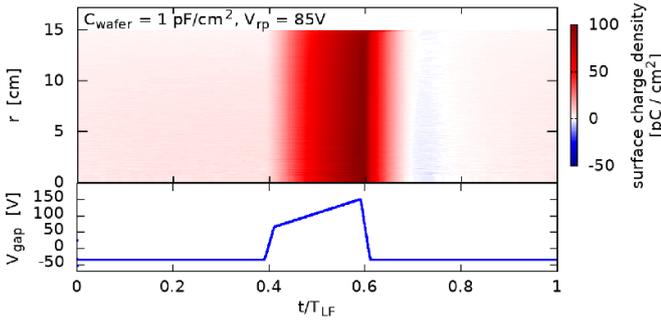
Figure 15. Time evolution of the radial surface charge distribution across the dielectric wafer. The voltage drop V_{gap} in the lower panel is measured between the conductive parts of the grounded and powered electrodes. Note the negative offset (DC self-bias) voltage with respect to the corresponding 1d3v data. Discharge conditions as in figure 14.
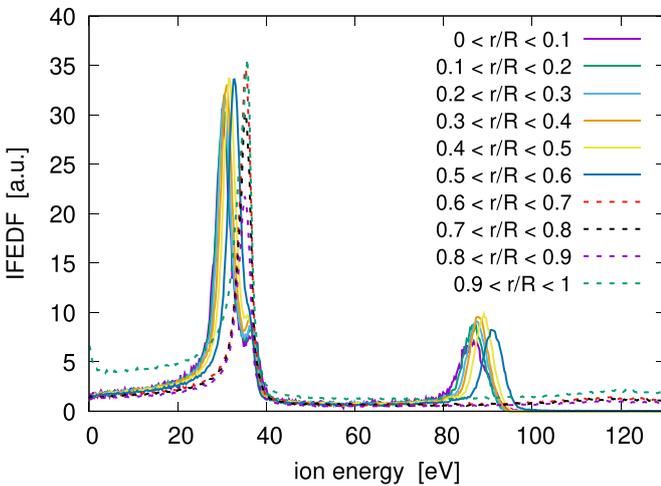

Figure 16. Radially resolved IFEDFs at the grounded side across the whole electrode area. Full lines correspond to the wafer surface, while dashed lines cover the conductive area of the electrode. Here $R = 251$ mm denotes the radial extent of the discharge chamber. Discharge conditions as in figure 14.

the chamber radius covering the wafer (solid lines) and the bare conductive part of the grounded electrode (dashed lines). Apparently, the compensation of the wafer charging and the reconstruction of the high energy peak can be achieved with the properly chosen ramp voltage at the whole wafer. The total flux does increase slightly (by approx. 10%–15%) with increasing radial position, and so does the spectral peak position but only by less than 5% over most of the wafer surface. At the rim of the wafer, at the outer few millimeters, the ion energy shows an additional increase by up to 10% with respect to the value at the center of the wafer.

4.2. Wafer on the powered side

Some applications may prefer to place the dielectric wafer on the powered electrode. In this case, the duty cycle has to be large ($D > 50$%) and the voltage ramp needs to be added to the negative portion of the LF voltage waveform to ensure
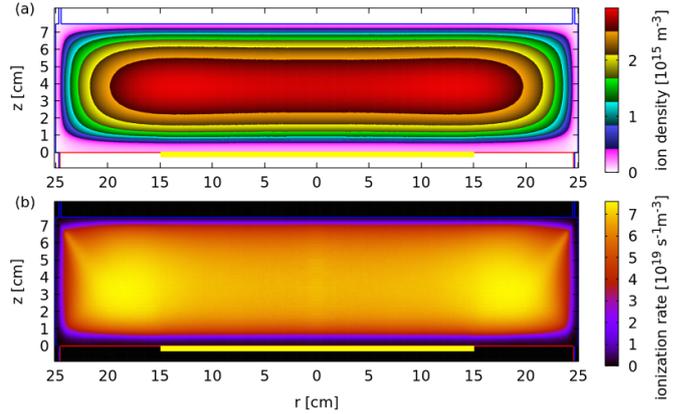

Figure 17. Spatial distribution of the time averaged Ar$^+$ ion density (a) and the ionization rate (b). Powered and grounded conductive surfaces are outlined with red and blue lines, respectively. The wafer with $C_{wafer} = 1$ pF cm^{-2} is marked with a thick yellow line embedded into the lower (powered) electrode. The voltage waveform parameters are: $V_{LF,pp} = 100$ V, $D = 80$%, $V_{rn} = 80$ V, and $V_{HF} = 92$ V.

the presence of a narrow high energy peak of the IFEDF at the wafer surface. Such a scenario is discussed in the following with discharge parameters $V_{HF} = 92$ V, $V_{LF,pp} = 100$ V, $V_{rn} = 80$ V, $C_{wafer} = 1$ pF cm^{-2}, and $D = 80$%.

The ion density profile, as shown in figure 17(a) is different than in the previous case, here the density does not peak in the center, and the maximum is displaced to the outer radii. The density modulation is not strong, the distribution above the wafer is practically homogeneous. The reason for the different density profiles can be identified from the distribution of the charged particle source function, as shown in panel (b). Similar to the previous case, we find enhanced ionization near the edge, however, the difference between the central region and the outer position is larger, apparently, the presence of the wafer reduces the plasma generation efficiency under these conditions in the center. During each HF cycle, there are two periods of peak ionization, which are the expansion phases of the powered and the grounded sheaths, separated by approx. 180° of the HF oscillation. Considering the fact that, with such low wafer capacitance, up to 8% of the HF voltage amplitude is absorbed by the wafer, effectively reducing the voltage drop between the wafer surface and the opposing electrode, we can expect a reduction of the ionization rate above the wafer with respect to the electrode surface not covered by the wafer. So far this is qualitatively valid for the previous case as well, however, the total area of the grounded plasma facing surface, including the electrode and the sidewalls, is much larger than the powered surface. Consequently, the ratio of conductive surface that is covered by the dielectric wafer is much smaller in the previous case, which results in a significantly weaker manifestation of the effective ionization rate reduction.

The time evolution of the radial surface charge distribution across the dielectric wafer in figure 18 shows a very homogeneous profile, except for the outermost few millimeters the charge variation develops equally over the whole surface.

J. Phys. D: Appl. Phys. **56** (2023) 055202

P Hartmann *et al*
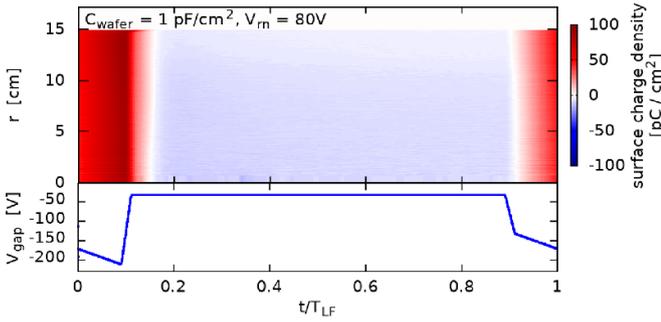
Figure 18. Time evolution of the radial surface charge distribution across the dielectric wafer. Discharge conditions as in figure 17.
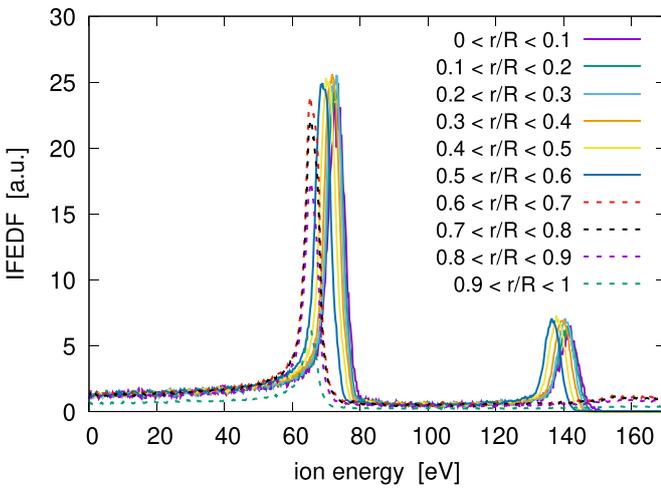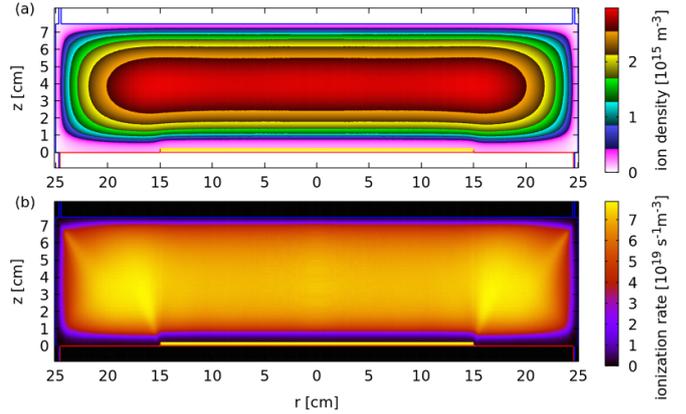

Figure 19. Radially resolved IFEDFs at the powered side across the whole electrode area. Full lines correspond to the wafer surface, while dashed lines cover the conductive area of the powered electrode. Discharge conditions as in figure 17.

Figure 20. Spatial distribution of the time averaged Ar^+ ion density (a) and the ionization rate (b). Powered and grounded conductive surfaces are outlined with red and blue lines, respectively. The wafer with $C_{wafer} = 1\,pF\,cm^{-2}$ and a width of $d = 2\,mm$ is marked with a thick yellow line on top of the lower (powered) electrode. The voltage waveform parameters are: $V_{LF,pp} = 100\,V$, $D = 80\%$, $V_{rn} = 80\,V$, and $V_{HF} = 92\,V$.

In this case, an even better degree of radial homogeneity can be seen in the radially resolved IFEDF data, as shown in figure 19. The IFEDFs are acquired for every decade of the chamber radius covering the wafer (solid lines) and the bare conductive part of the powered electrode (dashed lines). The compensation of the wafer charging and the reconstruction of the high energy peak can be achieved with a single negative ramp voltage at the wafer. The total ion flux is very stable across the whole wafer and the spectral peak position decreases only slightly (by about 5%) with increasing radius. The high energy peak in the IFEDF appears at approx. 140 eV, while in the previous case with the opposite geometry it was significantly lower (approx. 90 eV). This difference can be attributed to the formation of the DC self-bias voltage, which shifts the time averaged electric potential of the powered electrode towards negative values, causing an electrical asymmetry, which is a consequence of the geometrical asymmetry.

4.3. Wafer edge effect

Keeping the wafer at the powered electrode and all other discharge conditions identical to the previous case, here we introduce a finite width for the dielectric wafer with $d = 2\,mm$, which is now standing out of the electrode surface.

The Ar^+ ion density distribution, as seen in figure 20(a) is similar to the $d = 0\,mm$ case with a slightly more developed density maximum right outside the wafer edge at $r = 15\,cm^{-1}$. This can be explained based on the distribution of the ionization source, as shown in figure 20(b), which now features two beam-like features. The first, formed by the superposition of the vertical and horizontal expansions of the grounded side sheaths, originating in the chamber corner, was already present in the previous cases. However, due to the presence of another corner, formed by the horizontal powered electrode and the vertical edge of the dielectric wafer, the effect of the superposition of the powered sheath expansions causes the formation of another high energy electron beam during the opposite phase of the HF voltage oscillation. This additional increase of the ionization source at the outer radial position contributes to the formation of the observed structure of the plasma density distribution, which is, nevertheless, fairly homogeneous above the wafer surface.

To estimate the radial extent of the wafer area that can be influenced by the presence of the wafer edge we investigate a series of snapshots of the radial electric field distribution in the vicinity of the wafer edge. Figure 21 shows six subsequent time instances, one before, four during, and one right after the negative voltage pulse, centered around $t = 10\,\mu s$, that is responsible for the formation of the high energy ion population. The radial electric field during the long period between the short negative voltage pulses is stable, accelerating ions inwards but it barely extends 1–2 mm above the wafer from the edge. During the negative voltage pulse, the magnitude of the radial electric field first increases by a factor of 2–3, extends a few mm·s deeper above the wafer, but with the surface charging process progressing in time, a local reversal of the electric field at the wafer corner develops, which, however, is only present for less than a μs,
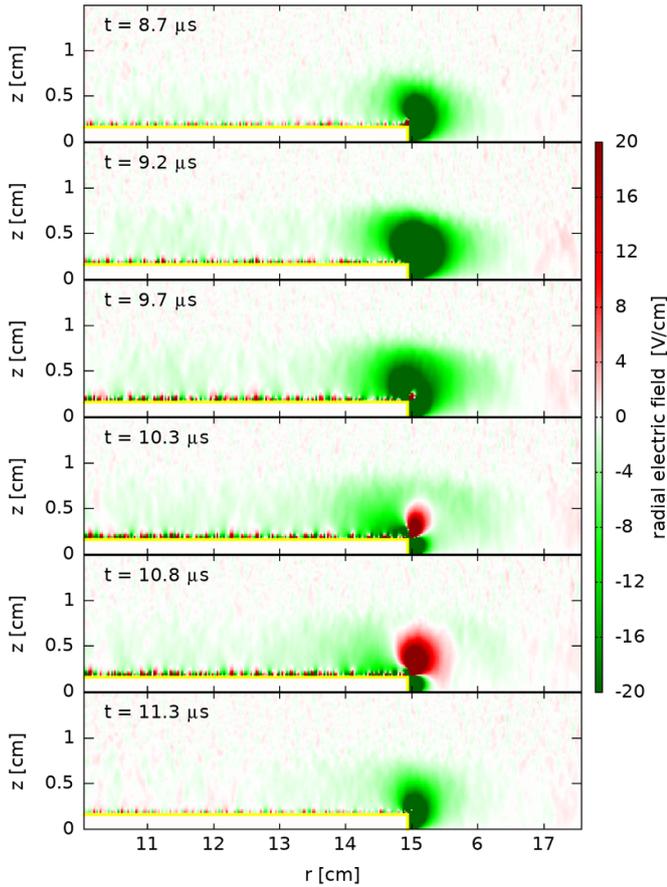
Figure 21. Snapshots of the radial electric field distribution. The negative voltage pulse is centered around $t = 10\,\mu s$ and is $2\,\mu s$ long. The yellow line shows the surface of the dielectric wafer. Discharge condition as in figure 20.

before the original, stable, inter-pulse field configuration is restored. At any time of this transition, the edge electric field does not propagate deeper than 5 mm above the wafer, meaning that the previously identified homogeneity of the plasma exposure across the whole 300 mm diameter wafer can be distorted only at the outermost few mm-s from the wafer edge.

5. Summary

In this numerical study, the interaction of low pressure capacitively coupled RF discharges (CCPs) in argon gas with dielectric substrate (wafer) surfaces was discussed. The possibility of the compensation of the surface charging effect by the application of tailored voltage waveforms was shown. A combination of a single HF (27.1 MHz) voltage signal and a LF (100 kHz) customized pulsed voltage waveform, including a base square voltage and constant slope ramp voltage components, has been used to generate IFEDFs with a narrow and controllable high energy peak at the wafer surface. Such IFEDFs are required to realize high selectivity and atomic layer precision in a variety of plasma processing applications. The effective recovery of the control over the IFEDF at the

dielectric wafer surface has been demonstrated. 1d3v and 2d3v PIC/MCC simulations have been developed and applied to perform a parametric investigation on the effect of the voltage waveform parameters on the plasma operation and the IFEDF at the wafer, as well as to reveal the radial distribution of the plasma exposure across the surface of a 300 mm diameter dielectric wafer, including edge effects. The conclusions of the present study are summarized as:

Dielectric wafers with low capacitance, $C_{\text{wafer}} \lesssim 10\,\text{pF}\,\text{cm}^{-2}$, can be charged to significant voltages during the different phases of the pulsed voltage signal that influence the time evolution of the electric field responsible for the ion acceleration towards the wafer surface, resulting in distortions of the IFEDFs.

Using duty cycles $D < 40\%$ and positive ramp voltages $V_{\text{rp}} > 0\,\text{V}$ high energy ion fluxes at the grounded side, while with $D > 60\%$ and negative ramp voltages $V_{\text{rn}} > 0\,\text{V}$ high energy ion fluxes towards the wafer at the powered side can be fine tuned. The parasitic effects of wafer charging, that lead to IFEDF distortion, can be compensated and the desired IFEDF shape can be restored by using such voltage ramps.

Varying the duty cycle of the LF pulsed waveform does only weakly influence the surface charging currents. Therefore, a constant slope of the voltage ramp can be used for different duty cycles to recover the narrow high energy peak in the IFEDFs.

The variation of the LF pulse amplitude does only marginally influence the plasma generation and with this the charged particle currents to the surfaces. Therefore, a single value of the ramp voltage can be used to recover the high energy peak in the IFEDFs for a wide range of voltage pulse amplitudes.

The amplitude of the HF cosine voltage signal strongly influences the plasma generation and the charged particle fluxes at the electrodes. The ramp voltage needs to be adjusted individually for every value of the HF voltage amplitude to restore the desired IFEDF shape.

In more realistic, geometrically asymmetric discharge conditions, the exact mirrored equivalence of the high- and low duty cycle waveforms is modified by the appearance of a geometry dependent shift of the DC self-bias voltage and edge effects in the charged particle generation.

The radial homogeneity of the ion fluxes and the IFEDFs are maintained within $\pm 10\%$ around the mean value for all quantities investigated. However, the small shifts in ion energy show different trends approaching the edge of the wafer for the cases with the wafer placed at the grounded or the powered electrode side.

The radial electric field developing at the edge of a wafer with finite thickness has a minor influence on the overall homogeneity of the plasma exposure of the whole wafer, its effect remains localized to the outermost few mm-s of the wafer.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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